We claim:

1. A method of forming an enhanced-surface-area conductive structure in the manufacture of a structure for use in an integrated circuit, the method comprising:

forming a layer containing at least two phases, the phases including at least one conductive phase; and

preferentially removing at least one of the at least two phases so as to leave behind at least the at least one conductive phase.

2. The method according to claim 1, wherein the act of removing comprises etching the layer.

3. The method of claim 1, wherein the act of forming comprises depositing the layer and annealing the layer.

4. The method of claim 1, wherein the act of forming comprises forming a layer having phases of ruthenium and of ruthenium oxide.

5. The method of claim 1, wherein the act of forming comprises depositing a layer of ruthenium oxide and annealing the layer of ruthenium oxide so as to form ruthenium and ruthenium oxide phases within the layer.

6. A method of forming a structure on an integrated circuit, the method comprising:

annealing a layer comprising oxygen-deficient non-stoichiometric conductive metallic oxide; and

removing metal from the annealed layer at a rate which is greater than the rate at which metallic oxide is removed from the layer.

7. The method of claim 6, wherein the act of annealing comprises annealing a layer comprising oxygen-deficient non-stoichiometric ruthenium oxide.

8. A method of forming a structure on an integrated circuit comprising:

at least partially separating a first layer into respective phases; and

differentially removing a first phase of the respective phases from the first layer, leaving a second phase of the respective phases within the first layer, wherein the second phase is an electrically conductive material.

9. The method according to claim 8, comprising:

providing a second layer of a dielectric material in proximity to the first layer; and

providing a third electrically conductive layer in proximity to the second layer.

10. The method according to claim 9, comprising abutting the first, second, and third layers against one another with no intermediate layers.

11. The method according to claim 8 in which the act of at least partially separating the first layer into respective phases comprises at least partially separating the first layer into respective ruthenium and ruthenium oxide phases.

12. A method of forming a conductive structure, comprising:

forming a layer of electrically conductive material;

forming a layer of non-stoichiometric ruthenium oxide on the layer of conductive material;

annealing the layer of non-stoichiometric ruthenium oxide to form ruthenium and ruthenium oxide phases; and

differentially removing the ruthenium phase relative to the ruthenium oxide phase.

13. The method of claim 12, wherein the non-stoichiometric ruthenium oxide layer is oxygen-deficient.

14. A method of forming a conductive structure, the method comprising:

depositing a layer of oxygen-deficient non-stoichiometric ruthenium oxide;

annealing the deposited layer for a time and at a temperature sufficient to cause at least some separation of ruthenium and ruthenium oxide phases within the layer; and

removing ruthenium preferentially over ruthenium oxide from the layer.

15. The method of claim 14, wherein the act of annealing comprises forming zones of ruthenium phase material within the layer with at least some of the zones extending through an entire thickness of the layer.

16. The method of claim 14, wherein the act of annealing comprises forming zones of ruthenium phase material within the layer, wherein a mean diameter of such zones is in the range of about one to about three times a thickness of the layer.

17. A method of forming a conductive structure, the method comprising:

forming a layer of electrically conductive material;

forming a layer of oxygen-deficient ruthenium oxide on the layer of conductive material;

annealing the layer of oxygen-deficient ruthenium oxide to form ruthenium and ruthenium oxide phases; and

differentially removing the ruthenium relative to the ruthenium oxide.

18. The method of claim 17, wherein the act of forming a layer of oxygen-deficient ruthenium oxide comprises depositing a layer of ruthenium oxide.

19. The method of claim 17, wherein the act of differentially removing comprises preferentially etching a ruthenium phase in a layer of oxygen-deficient ruthenium oxide and ruthenium.

20. A method of forming at least one capacitor in an integrated circuit, the method comprising:

forming a first conductive layer comprising ruthenium and ruthenium oxide phases;

removing ruthenium from the first conductive layer so as to leave remaining zones of ruthenium oxide;

forming a dielectric layer on or in proximity to the remaining zones of ruthenium oxide; and

forming a second conductive layer on or in proximity to the dielectric layer.

21. The method of claim 20, wherein the dielectric layer and second conductive layer are each a single layer of a homogenous material.

22. The method of claim 20, wherein the act of forming the dielectric layer comprises forming a layer of a material having a dielectric constant of at least 9.

23. The method of claim 20, wherein the act of forming the dielectric layer comprises forming a layer of a material having a dielectric constant of at least 20.

24. The method of claim 20, wherein the act of forming the dielectric layer comprises forming a layer of tantalum pentoxide.

25. A method of forming a capacitor, comprising:

forming a first layer of conductive material;

forming a second layer over the first layer of conductive material, the second layer comprising zones of ruthenium and ruthenium oxide;

etching the zones of ruthenium so as to allow the zones of ruthenium oxide to remain;

forming a layer of dielectric material on the remaining zones of ruthenium oxide and the first layer of conductive material; and

forming a third layer of conductive material on the layer of dielectric material.

26. The method of claim 25, wherein the act of forming a first layer comprises forming a first layer of conductive material resistant to the etching performed in the act of etching the zones of ruthenium.

27. The method of claim 25, wherein the act of forming the second layer comprises forming a layer of ruthenium oxide and at least partially separating the layer of ruthenium oxide into ruthenium oxide and ruthenium phases.

28. The method of claim 25, wherein the step of forming a layer of dielectric material comprises forming a layer of dielectric material conformally over the remaining zones of ruthenium oxide such that a surface of the layer of dielectric material spaced from the surface of the remaining zones of ruthenium oxide conforms at least in part to the contours of the surface of the remaining ruthenium oxide.

29. The method of claim 25, further comprising etching the zones of the ruthenium and ruthenium oxide to have a mean closest distance that is at least twice a thickness of the layer of dielectric material.

30. An enhanced-surface-area conductive structure in an integrated circuit, the structure comprising a layer of ruthenium oxide having at least one pitted surface.

31. A capacitor structure in an integrated circuit, the structure comprising a layer of conductive metallic oxide having a pitted surface with a layer of dielectric material disposed conformally on the pitted surface.

32. The capacitor structure of claim 31, further comprising a layer of conductive material disposed on the layer of dielectric material.

33. The capacitor structure of claim 31, wherein at least some of the pits in the surface of the conductive metallic oxide layer extend completely through the conductive metallic oxide layer.

34. The capacitor structure of claim 33, wherein the pits in the surface of the conductive metallic oxide layer have a mean diameter in the range of one to three times a thickness of the conductive metallic oxide layer.

35. The capacitor structure of claim 33, wherein the pits in the surface have a mean closest distance that is at least two times a thickness of the layer of dielectric material.

36. The capacitor structure of claim 31, wherein the conductive metallic oxide layer comprises ruthenium oxide.

37. A conductive structure in an integrated circuit, the structure comprising a layer of conductive material with islands of conductive metallic oxide disposed thereon.

38. The structure of claim 37, wherein the conductive metallic oxide comprises ruthenium oxide.

39. A capacitor structure in an integrated circuit, the structure comprising:

a layer of conductive material with islands of conductive metallic oxide disposed thereon; and

a layer of dielectric material disposed conformally on the islands of conductive metallic oxide, wherein a portion of a surface of the layer of conductive material is exposed between the islands.

40. The capacitor structure of claim 39, wherein the conductive metallic oxide comprises ruthenium oxide.

41. The capacitor structure of claim 39, further comprising a layer of conductive material disposed conformally on the layer of dielectric material.

42. An integrated circuit, comprising a plurality of capacitors that include a layer of conductive metallic oxide having a pitted surface with a layer of dielectric material disposed conformally on the pitted surface.